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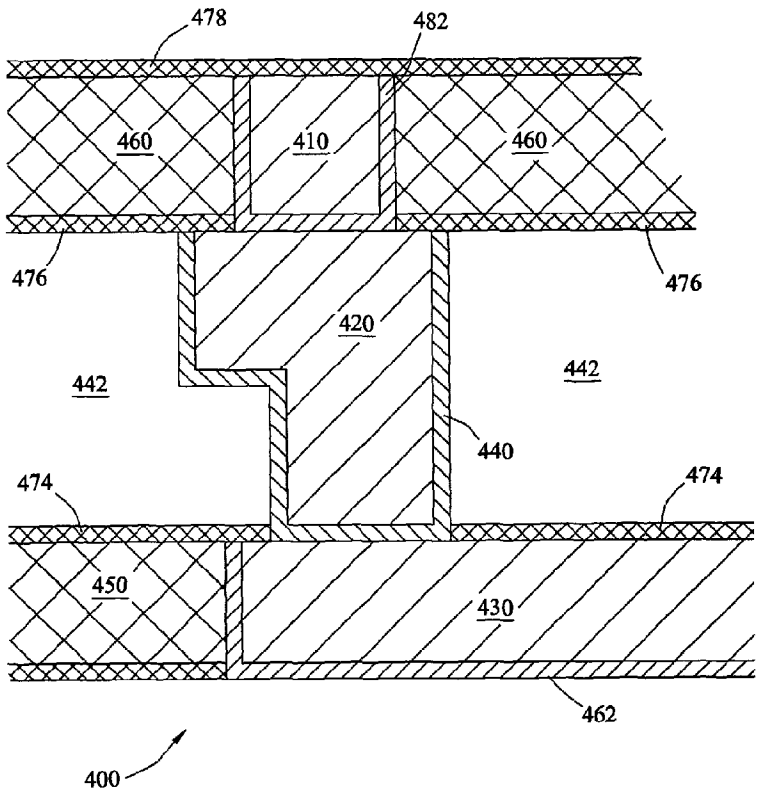
(54) Title: METHOD OF USING TERNARY COPPER ALLOY TO OBTAIN A LOW RESISTANCE AND LARGE GRAIN SIZE INTERCONNECT



(57) Abstract: A method of fabricating an integrated circuit includes forming a barrier layer along lateral side walls and a bottom of a via aperture and providing a ternary copper alloy via material in the via aperture to form a via. The via aperture is configured to receive the ternary copper alloy via material and electrically connect a first conductive layer and a second conductive layer. The ternary copper alloy via material helps the via to have a lower resistance and an increased grain size with staffed grain boundaries.

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METHOD OF USING TERNARY COPPER ALLOY TO OBTAIN A LOW RESISTANCE AND LARGE GRAIN SIZE INTERCONNECT

FIELD OF THE INVENTION

The present invention relates generally to integrated circuits and methods of manufacturing integrated circuits. More particularly, the present invention relates to a method of using ternary copper alloy to obtain a low resistance and large grain size interconnect.

BACKGROUND OF THE INVENTION

Semiconductor devices or integrated circuits (ICs) can include millions of devices, such as, transistors. Ultra-large scale integrated (ULSI) circuits can include complementary metal oxide semiconductor (CMOS) field effect transistors (FET). Despite the ability of conventional systems and processes to fabricate millions of IC devices on an IC, there is still a need to decrease the size of IC device features, and, thus, increase the number of devices on an IC. Nevertheless, there are many factors that make the continued miniaturization of ICs difficult. For example, as the size of vias (or pathways between integrated circuit layers used to electrically connect separate conductive layers) decreases, electrical resistance increases.

Conventional integrated circuits utilize vias to connect structures (e.g., gates, drain regions, source regions) and conductive lines. A via is typically a metal plug which extends through an insulative layer. A barrier layer is used to protect the via from metal diffusion and from electromigration (EM). The barrier layer can contribute significantly to resistance associated with the via metal. Electromigration is the mass transport due to momentum exchange between conducting electrons and diffusing metal atoms. Electromigration causes progressive damage to the metal conductors in an integrated circuit. In general, it is characteristic of metals at very high current density and temperatures of 100C or more.

Integrated circuit manufacturers have attempted to reduce via resistance as the via size decreases by reducing the thickness of the barrier material. According to one conventional process, plasma vapor deposition (PVD), IC manufacturers deposit a very thin barrier material at the bottom of the via due to non-conformed deposition. The thickness of the barrier material is reduced by chemical vapor deposition (CVD) or atomic layer deposition (ALD) processes. These advanced deposition processes form hightly conformed barrier metal films. However, reducing the barrier thickness causes the barrier to become more permeable to copper (Cu) diffusion, which can adversely affect resistance to electromigration.

FIGURES 1A and 1B illustrate a schematic cross-sectional view of a portion 100 of an integrated circuit including a copper layer 110, a copper via 120, a copper layer 130, a dielectric layer 150, and a dielectric layer 160. Via 120 and copper layer 130 are separated by a barrier layer 140.

Portion 100 also includes a dielectric layer 142 that is separated from copper layer 130 by an etch stop layer 174. Dielectric layer 142 can be oxide and etch stop layer 174 can be Silicon Nitride (SiN). Etch stop layer 174 prevents diffusion of copper from copper layer 130 into dielectric layer 142. Dielectric layer 150 can be separated from copper layer 130 by a barrier layer 152. Similarly, dielectric layer 160 can be separated from copper layer 110 by a barrier layer 182. Barrier layers 152 and 182 can be Tantalum Nitride (TaN). Etch stop layers 172, 174, 176, and 178 can be Silicon Nitride (SiN).

According to conventional processes, barrier layer 140 can have a cross-sectional thickness of between 7 nm to 25 nm. Barrier layer 140 inhibits diffusion of copper ions from layers into via 120 and from via into dielectric layer 142. Conventional barrier layers can include Tantalum Nitride (TaN).

FIGURE 1A shows a portion formed according to a single damascene process where copper layer 110 and copper via 120 are deposited in two separate steps and are separated by a barrier section 182. FIGURE 1B shows a portion formed according to a dual damascene process where copper layer 110 and copper via 120 are deposited in one step or process and are not separated by a barrier.

As discussed above, conventional systems have attempted to reduce the thickness of barrier layer 140 to reduce the resistance associated with via 120. However, this reduction in thickness can cause electromigration failures. FIGURES 2A and 2B illustrate portion 100 described with reference to FIGURES 1A and 1B, further having an EM failure or void 145 in copper layer 130. FIGURE 2A shows a portion formed according to a single damascene process (as described with reference to FIGURE 1A) where copper layer 110 and copper via 120 are formed in two separate steps or processes. FIGURE 2B shows a portion formed according to a dual damascene process (as described with reference to FIGURE 1B) where copper layer 110 and copper via 120 are formed in one step or process.

FIGURES 3A and 3B illustrate portion 100 having an EM failure or void 155 in via 120 due to copper diffusion from copper via layer 120. FIGURE 3A shows a portion formed according to a single damascene process (as described with reference to FIGURE 1A) where copper layer 110 and copper via 120 are formed in two separate steps or processes. FIGURE 3B shows a portion formed according to a dual damascene process (as described with reference to FIGURE 1B) where copper layer 110 and copper via 120 are formed in one step or process.

EM failures have been described by Stanley Wolf, Ph.D. in Silicon Processing for the VLSI Era, Lattice Press, Sunset Beach, California, Vol. 2, pp. 264-65 (1990). Dr. Wolf explains that a positive divergence of the motion of the ions of a conductor leads to an accumulation of vacancies, forming a void in the metal. Such voids may ultimately grow to a size that results in open-circuit failure of the conductor line.

Thus, there is a need for an interconnect or via having less resistance while not experiencing electromigration in via or line failures. Further, there is a need for a method of forming a large grain size

interconnect having staffed grain boundaries for high electromigration reliability. Even further, there is a need for a method of using ternary copper alloy to obtain a low resistance and large grain size interconnect.

SUMMARY OF THE INVENTION

An exemplary embodiment is related to a method of fabricating an integrated circuit. This method can include forming a barrier layer along lateral side walls and a bottom of a via aperture and providing a ternary copper alloy via material in the via aperture to form a via. The via aperture is configured to receive the ternary copper alloy via material and electrically connect a first conductive layer and a second conductive layer. The ternary copper alloy via material helps the via have a lower resistance and an increased grain size.

Another exemplary embodiment is related to a method of using ternary copper alloy to obtain a low resistance and large grain size interconnect or via. This method can include providing a first conductive layer over an integrated circuit substrate, providing a conformal layer section at a bottom and sides of a via aperture positioned over the first conductive layer to form a barrier separating the via aperture from the first conductive layer, filling the via aperture with a ternary copper alloy via material to form a ternary copper alloy via, and providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer to the second conductive layer.

Another exemplary embodiment is related to a method of forming a via in an integrated circuit. This method can include depositing a first conductive layer, depositing an etch stop layer over the first conductive layer, depositing an insulating layer over the etch stop layer, forming an aperture in the insulating layer and the etch stop layer, providing a barrier material at a bottom and sides of the aperture to form a barrier layer, filling the aperture with a ternary copper alloy via material to form a ternary copper alloy via, and providing a second conductive layer over the ternary copper alloy via such that the ternary copper alloy via electrically connects the first conductive layer and the second conductive layer.

Other principle features and advantages of the invention will become apparent to those skilled in the art upon review of the following drawings, the detailed description, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements, and:

FIGURE 1A is a schematic cross-sectional view representation of a single damascene portion of an integrated circuit fabricated in accordance with prior art;

FIGURE 1B is a schematic cross-sectional view representation of a dual damascene portion of an integrated circuit fabricated in accordance with prior art;

FIGURE 2A is a schematic cross-sectional view representation of the single portion of the integrated circuit illustrated in FIGURE 1A, showing an electromigration failure;

FIGURE 2B is a schematic cross-sectional view representation of the dual portion of the integrated circuit illustrated in FIGURE 1B, showing an electromigration failure;

FIGURE 3A is a schematic cross-sectional view representation of the single damascene portion of the integrated circuit illustrated in FIGURE 1A, showing an electromigration failure;

FIGURE 3B is a schematic cross-sectional view representation of the dual damascene portion of the integrated circuit illustrated in FIGURE 1B, showing an electromigration failure;

FIGURE 4 is a schematic cross-sectional view representation of a portion of an integrated circuit, showing a ternary copper alloy interconnect in accordance with an exemplary embodiment;

FIGURE 5 is a top cross-sectional view representation of a portion of an integrated circuit, showing a ternary copper allow interconnect structure in accordance with another exemplary embodiment;

FIGURE 6 is a schematic cross-sectional view representation of a portion of an integrated circuit, showing a ternary copper alloy interconnect in accordance with another exemplary embodiment; and

FIGURE 7 is a schematic cross-sectional view representation of a portion of an integrated circuit, showing a ternary copper alloy interconnect in accordance with yet another exemplary embodiment.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

With reference to FIGURE 4, a schematic cross-sectional view representation of a portion 400 of an integrated circuit includes a conductive via layer 410, a conductive layer and via section 420, a conductive layer 430, a barrier layer 440, a dielectric layer 450, and a dielectric layer 460. Portion 400 is preferably part of an ultra- large-scale integrated circuit having millions or more transistors. Portion 400 is manufactured as part of the IC on a semiconductor wafer, such as, a silicon wafer.

Portion 400 can also include a dielectric layer 442 that is separated from conductive layer 430 by an etch stop layer 474. In an exemplary embodiment, dielectric layer 442 is an oxide material and etch stop layer 474 is Silicon Nitride (Si_3N_4) or other suitable material. Etch stop layer 474 prevents diffusion of materials from conductive layer 430 into dielectric layer 442. Conductive via layer 410 can be a layer of any conductive material, such as, copper or another metal.

Dielectric layer 450 can be separated from copper layer 430 by a barrier layer 452. Similarly, dielectric layer 460 can be separated by copper layer 410 by a barrier layer 482. Barrier layers 452 and 462 can be Tantalum Nitride (TaN). Etch stop layers 472, 474, 476, and 478 can be Silicon Nitride (SiN).

Conductive layer and via section 420 can be made of a conductive material and serves to electrically connect conductive layer 410 and conductive layer 430. Conductive layer and via section 420 can include a ternary copper (Cu) alloy, Cu-X-Y. X can be any of a variety of elements with a characteristic of lowering resistance, such as, Zinc (Zn), Silver (Ag), or Tin (Sn). Y can be any of a variety of elements with a characteristic of increasing grain size, such as, Calcium (Ca) or Chromium (Cr).

Advantageously, the ternary copper alloy of via section 420 provides a low resistance interconnect or via, large grain size interconnect, and staffed grain boundaries. Large grain size promote electromigration reliability because the crystal structure interferes with the mobility of the copper ions. Large grain size also provides lower interconnect resistance. Staffed grain boundaries increase electromigration reliability because of reduction or restriction of Cu diffusion pathways along grain boundaries.

The material of conductive layer and via section 420 can be deposited using ECD (electrochemical deposition) – either electroless and/or electroplating. A seed layer for the electrochemical deposition can be formed by ALD/CVD (atomic layer deposition / chemical vapor deposition) and/or PVD/IMP (plasma vapor deposition / ion metal plasma), SIP (self-ionizing plasma). As an example, the ternary copper alloy of Cu-X-Y can be Cu-Sn-Cr where Tin (Sn) is less than 1 atomic % and Chromium (Cr) is less than 1 atomic %. As another example, Cu-X-Y can be Cu-Zn-Cr where Zinc (Zn) is less than 1 atomic % and Chromium (Cr) is less than 1 atomic %. In the case of Cu-Zn-Cr, the reduced resistance can be 1.8 – 2.2 $\mu\Omega$ cm and the increased grain size can be 0.5 – 3 μm.

An electroplating solution for Cu-Zn-Cr alloy deposition can include Cu salt as a Cu ion source, Zn salt as a Zn ion source, Cr salt as a Cr ion source, complexing agents for metallic ions, pH adjuster, and organic additives. Concentrational ratios of the metallic ions in solution are optimized to form Cu-Zn-Cr films with less than 1 atom % of Zn and Cr in the alloy film. Complexing agents can be selected from the group of ethylenediamine, ethylenediaminetetraacetic acid, and tartaric acid. Organic additives are selected from the group of polypropylene glycoles, polyethylene glycoles and mercaptan disulfides providing favorable conditions for shape evolution in via/trench area to complete Cu-Zn-Cr fill and to form conductive via layer without voids.

Anneal of electroplated Cu-Zn-Cr layer can be performed to complete recrystallization process further resulting in increased grain size and lowered resistance.

Chemical mechanical polishing, chemical polishing and/or electropolishing can be used to remove Cu-Zn-Cr and barrier layer from the dielectric forming planar surface ready for the next dielectric layer deposition.

Conductive layer 430 can be a layer of copper positioned in proximate location to via section 420. Conductive layer 430 can include an alloy including copper (Cu). In an alternative embodiment, conductive layer 430 is a stack of several layers.

Barrier layer 440 can be Tantalum (Ta), Tantalum Nitride (TaN) Titanium Nitride (TiN), Titanium Silicon Nitride (TiSiN), Tungsten Nitride (WNx), or other suitable material. In an exemplary embodiment, barrier layer 440 has a cross-sectional thickness of 5-10 nm. In other embodiments, barrier layer 440 can have dimensions as small as 2-5 nm.

In an exemplary dual damascene method of fabricating portion 400, once conductive layer 430 is deposited, etch stop layer 474 is deposited over conductive layer 430 and dielectric layer 442 is deposited over etch stop layer 442. A resist layer is deposited over dielectric layer 442 and is used in the patterning and etching of an aperture in dielectric layer 442 and etch stop layer 474 in the formation of via section 420. In an exemplary embodiment where via and trench sections have two different widths, two different resist layers can be used in a two step via/trench formation process. The resist layer or layers are removed before depositing via/trench material in conductive layer and via section 420. Conductive via layer 410 is formed to electrically connect conductive layer 420.

Referring to FIGURE 5, a portion 500 of an integrated circuit includes a dual damascene via/trench section having a ternary copper alloy. Via/trench section can include increased grain sizes 520, reduced resistance and staffed grain boundaries 510 due to the addition of Tin (Sn) and Chromium (Cr). With increased grain, size, staffed grain boundaries 510 and reduced resistance, via/trench section can have improved electromigration reliability. As described with respect to FIGURE 4, a variety of different techniques can be employed to include elements that lower resistivity and elements that increase grain size. A variety of different elements and combinations of elements can also be used.

FIGURE 6 illustrates a schematic cross-sectional view representation of a dual damascene portion 600 of an integrated circuit (IC), including a conductive layer 610, a via/trench section 620, a conductive layer 630, a barrier layer 640, a dielectric layer 650, and a dielectric layer 660. Portion 600 also includes a dielectric layer 642 that is separated from conductive layer 630 by an etch stop layer 644. Portion 600 is similar to portion 400 described with reference to FIGURE 4 with the exception of via/trench section 620 having a shape of a wide interconnect, compared to shape of via/trench section 420 of narrow interconnect.

Dielectric layers can include low dielectric constant materials deposited by CVD or spin-on techniques. Low dielectric constant materials can have dielectric constant $k = 1.5\text{-}3.5$ and can include porous materials with porosity between 10 and 45%. Pore size can have dimensions of 1-15 nm.

Dielectric layer 650 can be separated from copper layer 630 by a barrier layer 652. Similarly, dielectric layer 660 can be separated from copper via layer 610 by a barrier layer 682. Barrier layers 652 and 682 can be Tantalum Nitride (TaN). Etch stop layers 672, 674, 676, and 678 can be Silicon Nitride (SiN).

FIGURE 7 illustrates a schematic cross-sectional view representation of a single damascene portion 700 of an integrated circuit, including a conductive layer 710, a via section 720, a conductive layer 730, a barrier layer 740, a dielectric layer 750, and a dielectric layer 760. Portion 700 also includes a dielectric layer 742 that is separated from conductive layer 730 by an etch stop layer 744.

Advantageously, use of a ternary copper alloy in the formation of vias or interconnects can provide improved reliability and performance. For example, electromigration reliability can be improved due to staffed grain boundaries. Further, electromigration is improved due to increased grain size.

While the exemplary embodiments illustrated in the figures and described above are presently preferred, it should be understood that these embodiments are offered by way of example only. Other embodiments may include, for example, different methods of implanting copper alloys and different elements into alloys. The invention is not limited to a particular embodiment, but extends to various modifications, combinations, and permutations that nevertheless fall within the scope and spirit of the appended claims.

WHAT IS CLAIMED IS:

1. A method of fabricating an integrated circuit (400), the method comprising:

forming a barrier layer (440) along lateral side walls and a bottom of a via aperture, the via aperture being configured to receive a via material that electrically connects a first conductive layer (410) and a second conductive layer (430); and

providing a ternary copper alloy via material in the via aperture to form a via (420).

2. A method of using ternary copper alloy to obtain a low resistance and large grain size interconnect or via, the method comprising:

providing a first conductive layer (430) over an integrated circuit substrate;

providing a conformal layer section (440) at a bottom and sides of a via aperture positioned over the first conductive layer (430) to form a barrier separating the via aperture from the first conductive layer (430);

filling the via aperture with a ternary copper alloy via material to form a ternary copper alloy via (420); and

providing a second conductive layer (410) over the ternary copper alloy via (420) such that the ternary copper alloy via (420) electrically connects the first conductive layer (410) to the second conductive layer (430).

3. The method of claim 1 or 2, wherein the ternary copper alloy via material includes an element with a characteristic for lowering resistance.

4. The method of claim 3, wherein the element with a characteristic for lowering resistance is Zinc (Zn), Silver (Ag), or Tin (Sn).

5. The method of claim 3, wherein the element with a characteristic for lowering resistance is one atomic percent or less of the ternary copper alloy via material.

6. The method of claim 1 or 2, wherein the ternary copper alloy via material includes an element with a characteristic for increasing grain size.

7. The method of claim 6, wherein the element with a characteristic for increasing grain size is Calcium (Ca) or Chromium (Cr).

8. The method of claim 6, wherein the element with a characteristic for increasing grain size is one atomic percent or less of the ternary copper alloy via material.

9. The method of claim 6, wherein the grain size is between 0.5 and 3.0 μm.

10. The method of claim 2, wherein the ternary copper alloy via material comprise CuAgCr, CuSnCa, CuZrCa, or CuAgCa.

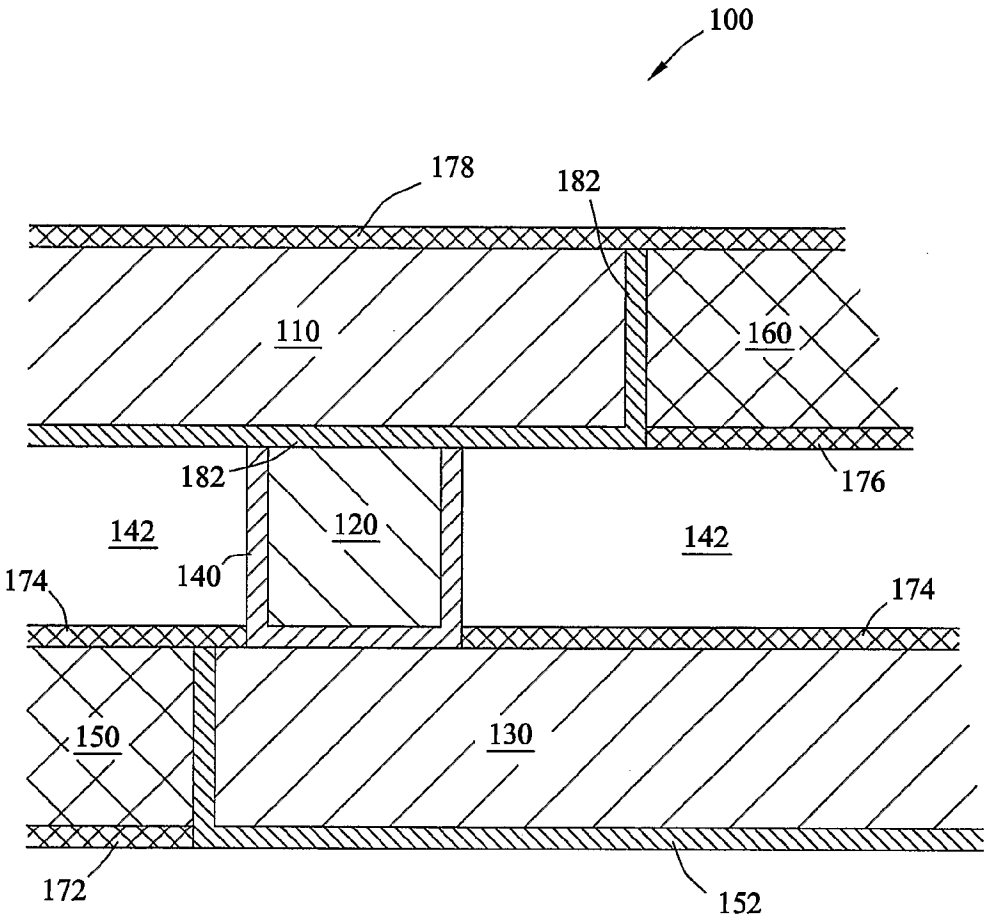
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FIG. 1A

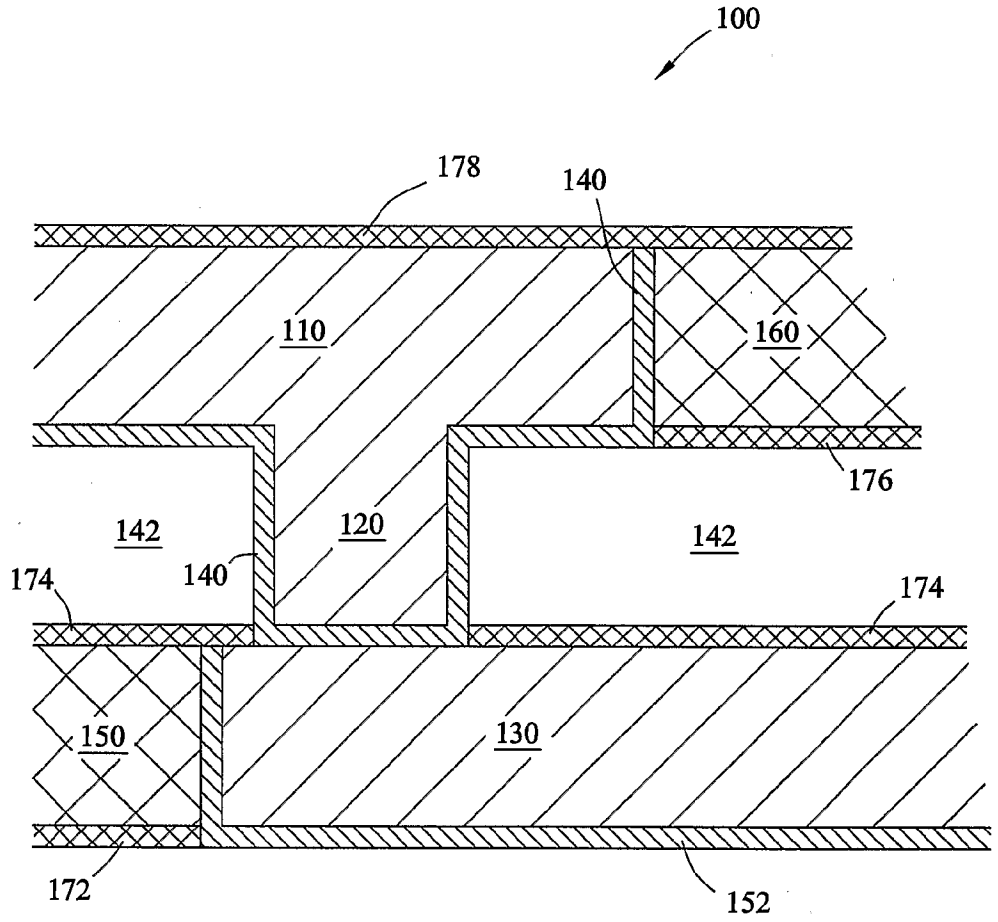
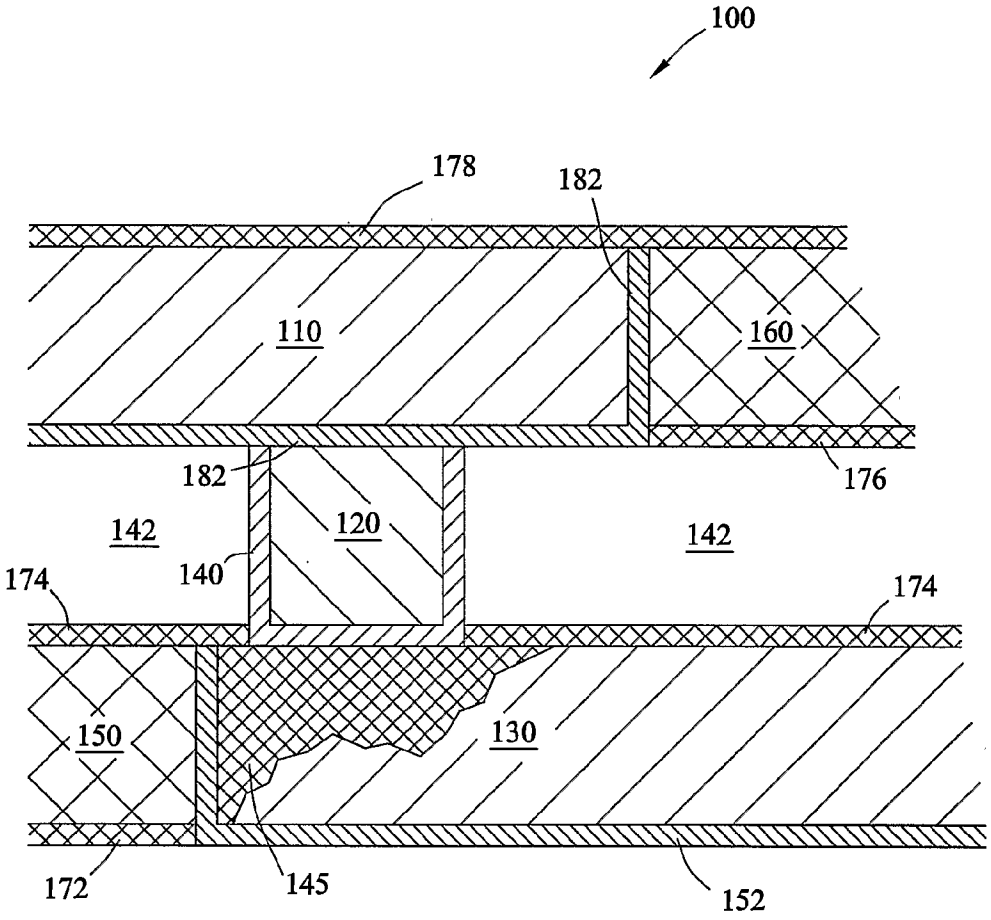


FIG. 1B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110
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182
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174
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FIG. 2A

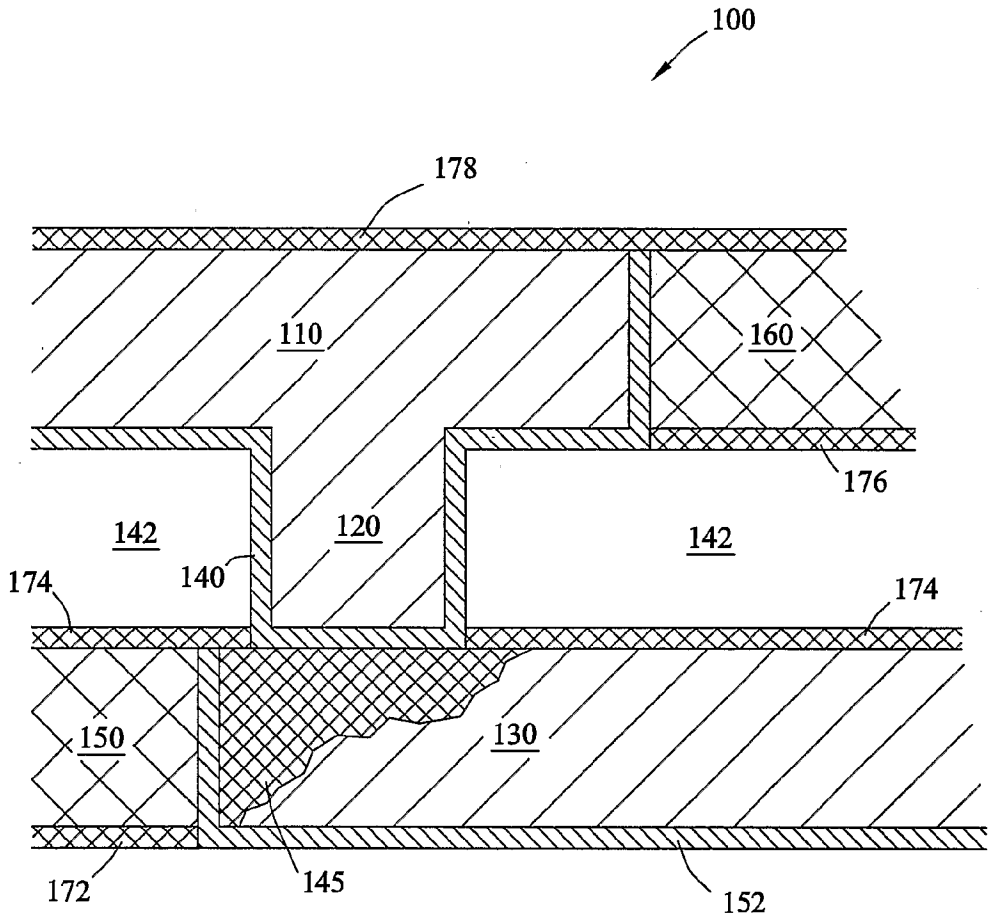
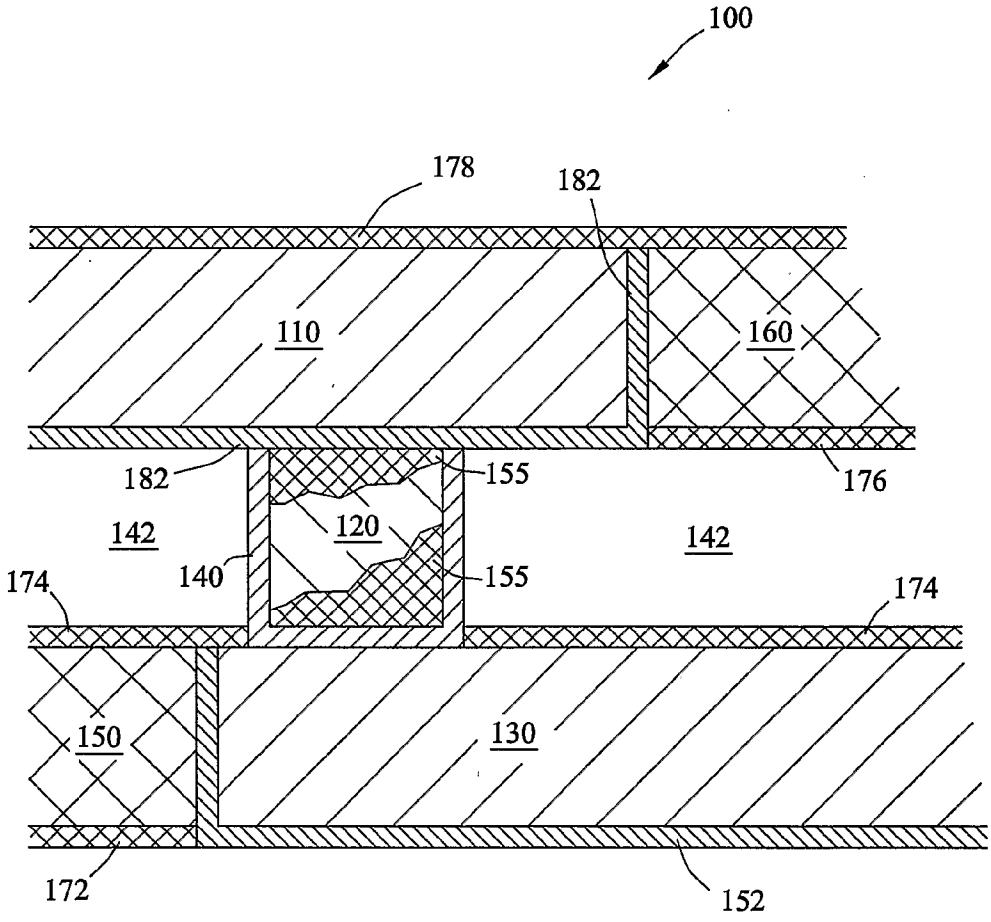


FIG. 2B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110
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182
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172
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FIG. 3A

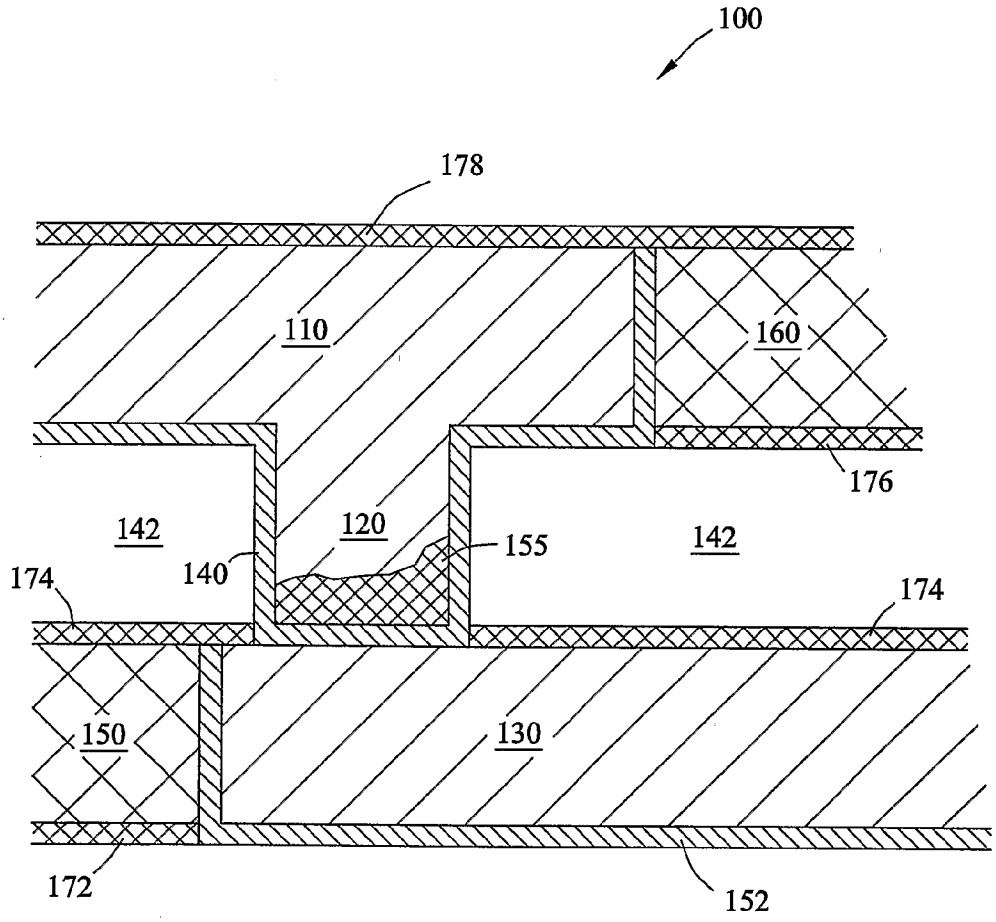
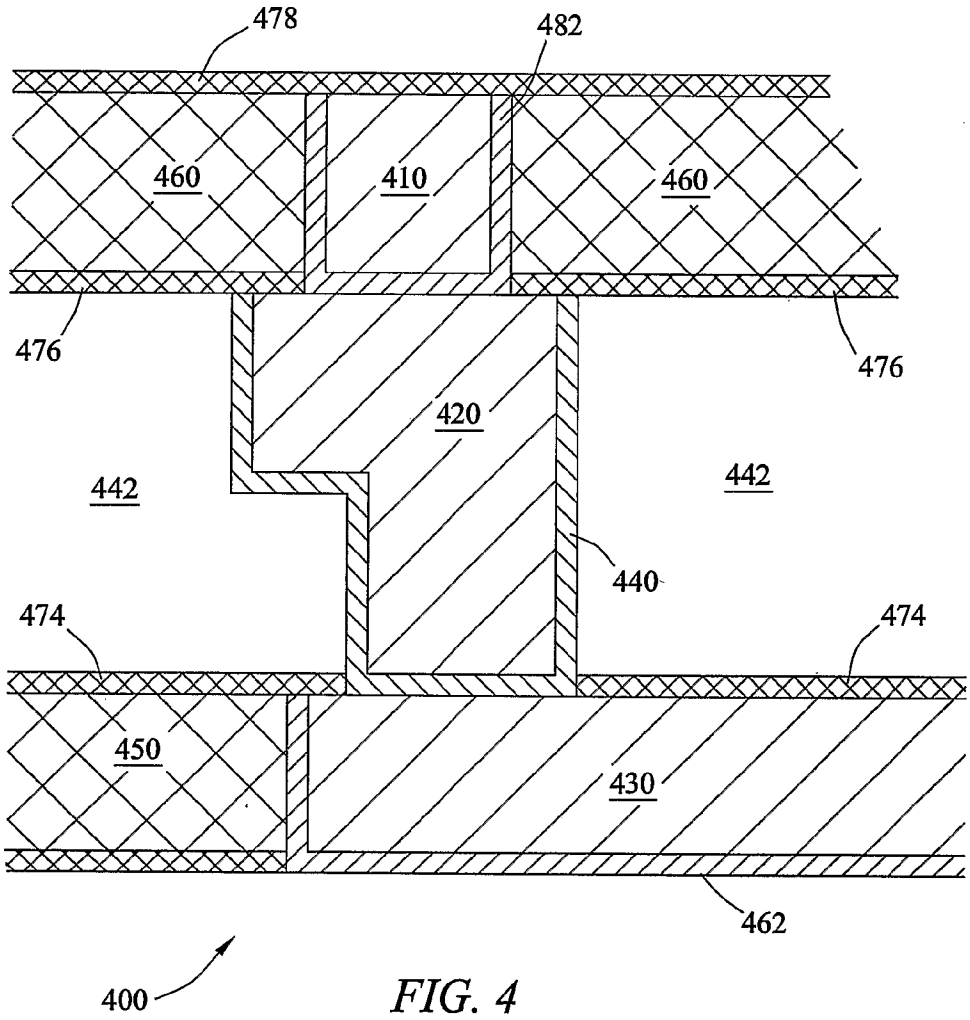


FIG. 3B


478
482
460
410
460
476
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420
442
442
440
474
474
450
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462
400

FIG. 4

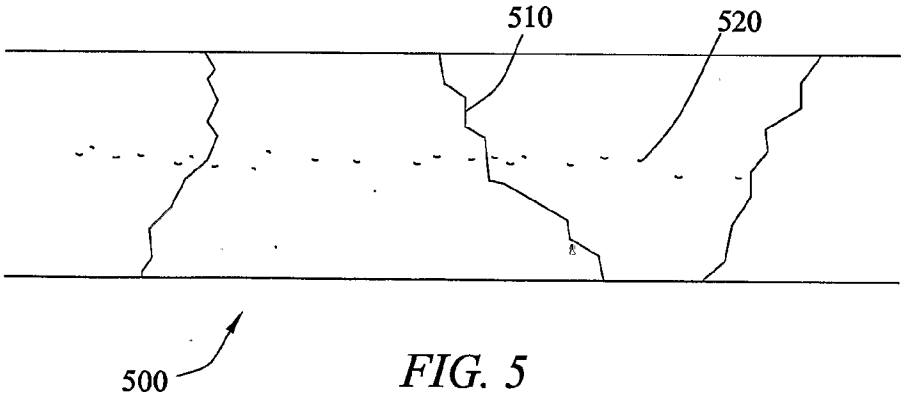
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FIG. 5

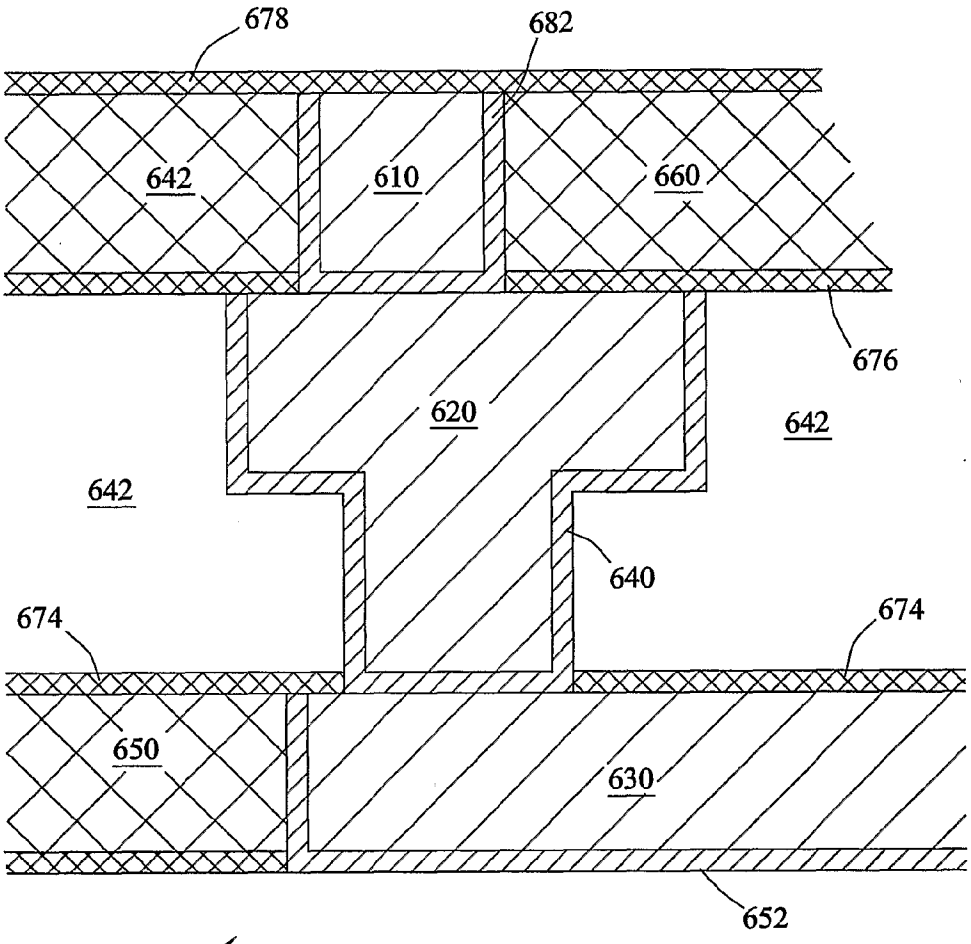

FIG. 6

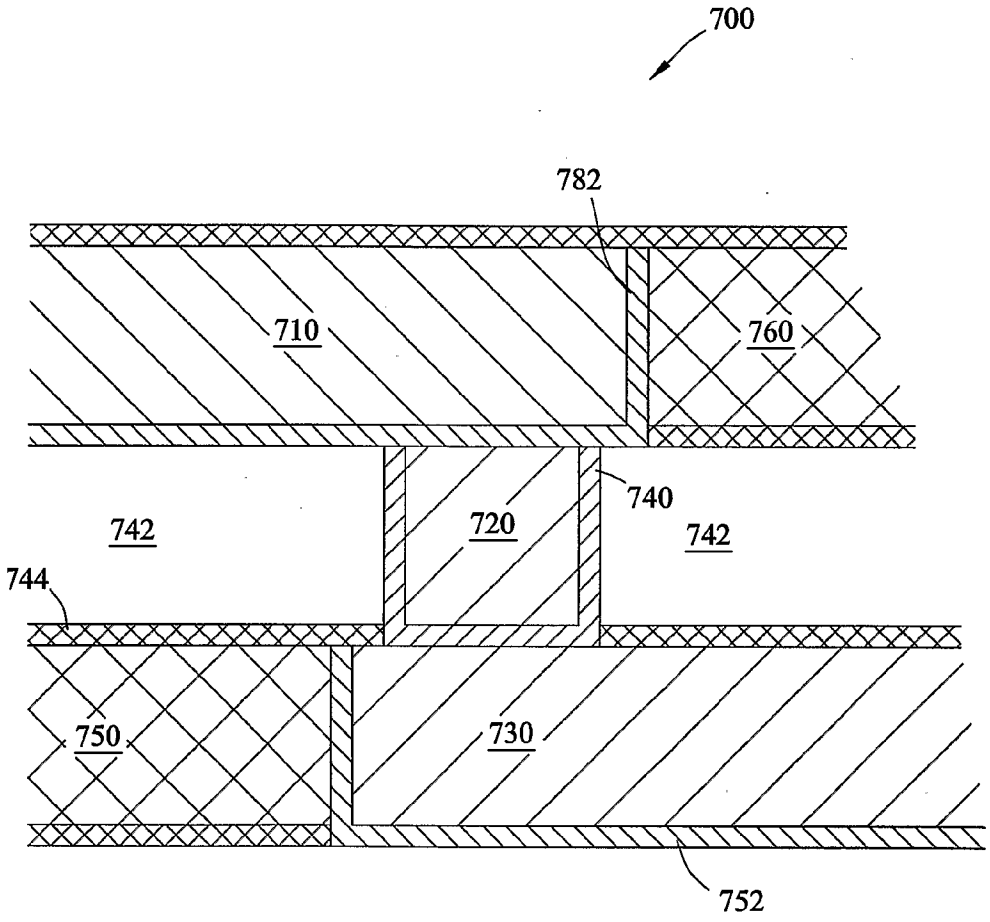

FIG. 7